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Low Power D Flip Flop Using Static Pass Transistor Logic

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***Abstract*: Minimizing power consumption is vitally important in modern circuit designs. The internal components should be designed in such a way that they consume low power with high speed. Flip flops are the storage elements in all digital design but, consume much power due to static and dynamic power dissipation and clock skew. The main idea is to introduce the design of high performance pass transistor flip flop which acquires less area and transistor count. In the existing method, an extremely low power flip flop named topologically compressed flip flop is proposed. As compared with conventional type FFs, the FF reduces power dissipation by 75% at 0% data activity. The reduction is achieved by merging the logically equivalent transistors to the unconventional latch structure. In order to reduce the transistor count and power consumption, a new method static pass transistor logic (SPTL) is introduced. The SPTL will be reducing the transistor count and power dissipation. The high performance of SPTL is designed and the simulation has been carried out on Tanner EDA Tool. An experimental chip design with 40 nm CMOS technology shows that almost all conventional FFs are replaceable with proposed FF while preserving the same system performance and layout area.**

***Keywords:* Flip flops, transistors, low power.**

1. INTRODUCTION

Power reduction in an IC is a grave concern in now days. With the increasing level of device integration and the growth in complexity of microelectronic circuits, power dissipation, delay and area has come the primary design goal. As the MOS devices are wide spread, there is high need for circuits which consume less power, mainly for convenient devices which run on batteries, like Laptops and hand-held computers. In LSI, generally more than half of the power is dissipated in random logic, of which half of the power is dissipated by flip-flops (FFs). As flip-flops are the major sector of the memory elements used in any portable devices, the major concern to reduce the power consumption in flip-flops will help us to reduce the power consumption in an IC to a major extent.

Flip-flops are used as the memory elements which are the basic building blocks of an IC. They are used in many applications like parallel data storage, shift registers, frequency division and counters etc. The purpose of this paper is to present a solution to achieve all of the goals: power reduction, transistor count, switching activity in the circuit and cell area.

In Section II, we review existing low-power FFs. In Section III, we show our design approach. In Section IV, we propose FF realization with a new methodology. In Section V, the detailed power and performance characteristics are shown compared to other FFs. In Section VI, we show the effect of the proposed FF in actual chip design by experimental layout.

II. LITERATURE SURVEY

In this section, the papers evaluate problems on previously report typical low-power FFs with comparison to a conventional FF shown in Fig. 1.

However, in actual chip design, the conventional FF is still used most often as a preferred FF because of its well-balanced power, performance and cell area.

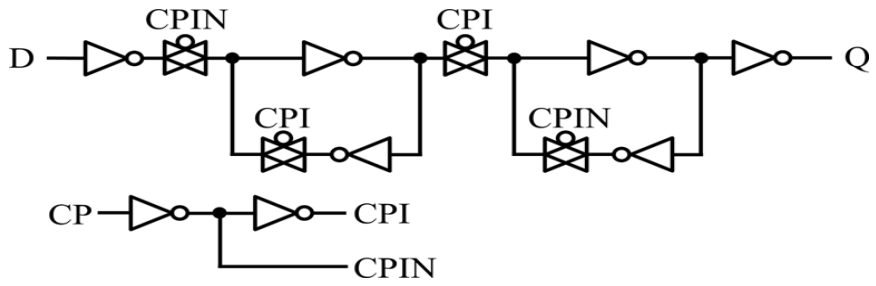

Fig.1. Conventional transmission-gate flip-flop

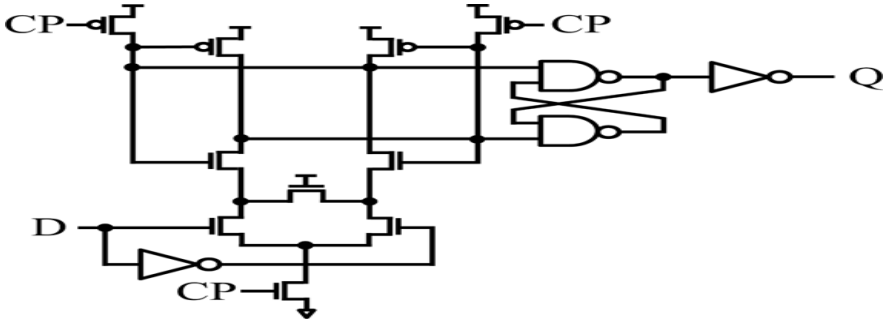

Fig: 2. Differential sense-amplifier flip-flop

Fig. 2 shows a characteristic circuit of differential sense-amplifier type FF. This type of circuit is very effective to amplify small-swing signals, so in general used in output of memory circuits.

In this FF, however, the result of power reduction goes down in the condition of lower data activity, because these kinds of circuits have pre-charge operation in every clock-low state. Moreover, if we use reduced clock swing, a modified clock generator and an extra bias circuit are necessary.

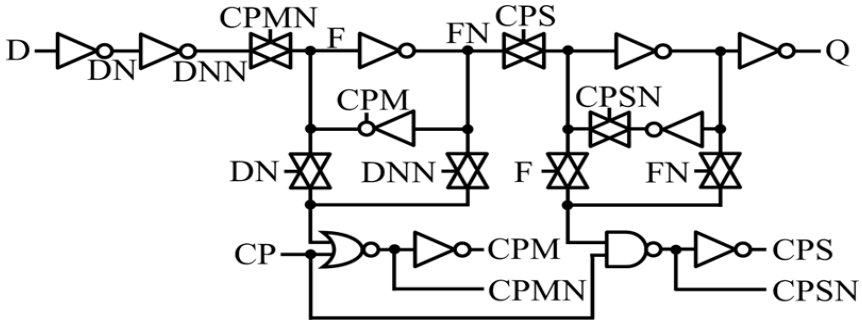

Fig. 3. Conditional-clocking flip-flop

Fig. 3 shows a circuit of conditional-clocking type FF. This circuit is achieved from a practical point of view. The circuit monitors input data change in every clock cycle and disables the operation of internal clock if input data are not altered. By this operation, power is concentrated when input data are not changed. But unfortunately, its cell area becomes almost twice that of the conventional circuit shown in Fig. 1.

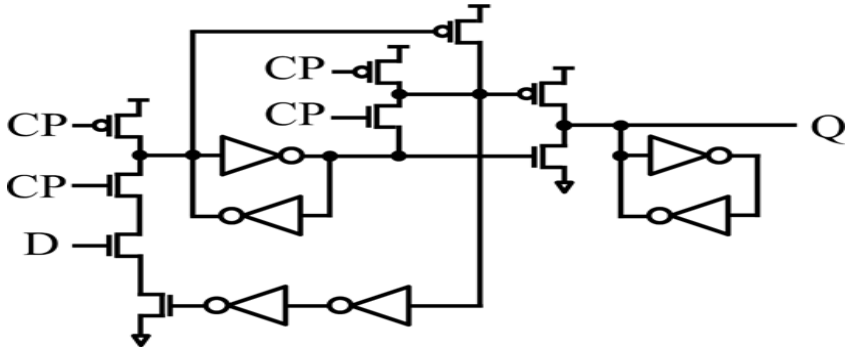

Fig. 4. Cross-charge control flip-flop (XCFF).

Fig. 4 shows the circuit of cross-charge control Flip flop. The feature of this circuit is to drive output transistors independently in order to reduce charged and discharged gate capacitance. However, in actual operation, some of the internal nodes are pre-set with clock signal in the case of data is high, and this operation dissipates additional power to charge and discharge internal nodes.

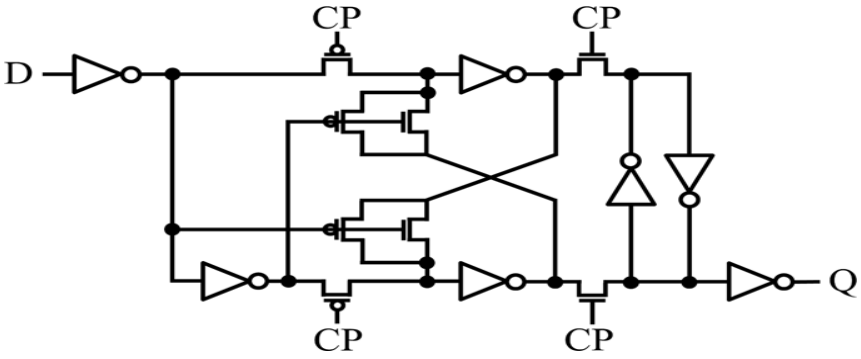

Fig. 5. Adaptive-coupling flip-flop (ACFF)

The adaptive-coupling type Flip Flop, shown in Fig. 5, is on a 6-transistor based memory cell.

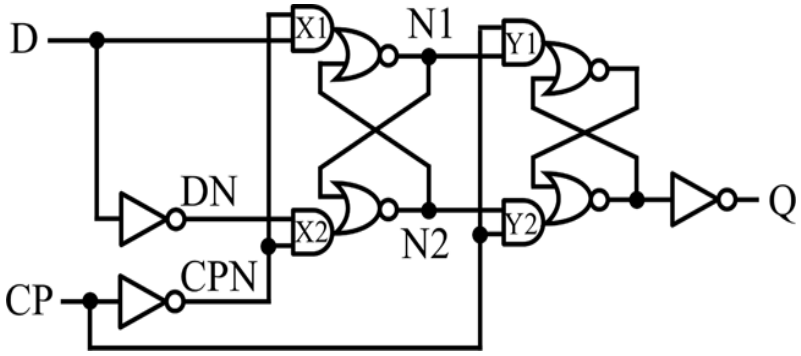

Fig. 6. Example of combinational type FF

In existing system conventional type flip flop is preferred FF because of its well impartial power, performance and cell area. In a conventional D Flip Flop, the clock signal always flows into the D flip-flop irrespective of whether the input changes or not. Part of the clock energy is consumed by the internal clock buffer to control the transmission gates without need. Hence, if the input of the flip-flop is the same to its output, the switching of the clock can be suppressed to conserve power.

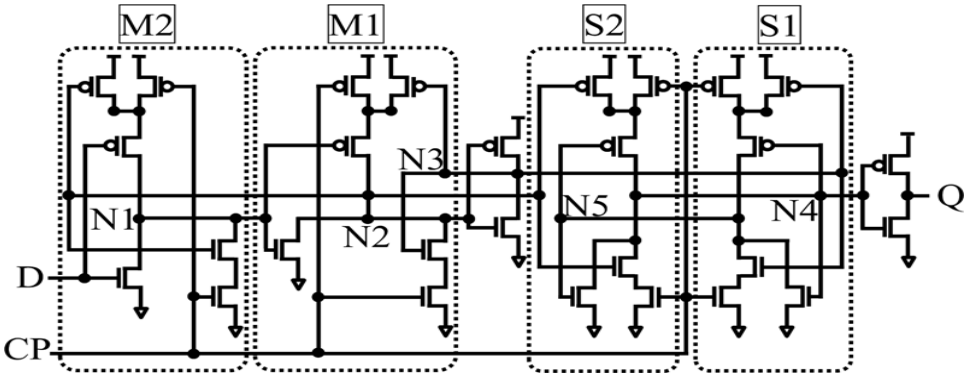

Fig. 8. Transistor level schematic of Fig. 7

To reduce the transistor-count based on logical equivalence, we consider a method consisting of the following two steps. As the first step, we plan to have a circuit with two or more logically equivalent AND or OR logic parts which have the same input signal combination, especially including clock signal as the input signals.

Then, merge those parts in transistor level as the second step.

IV. TOPOLOGICALLY COMPRESSD FLIP FLOP

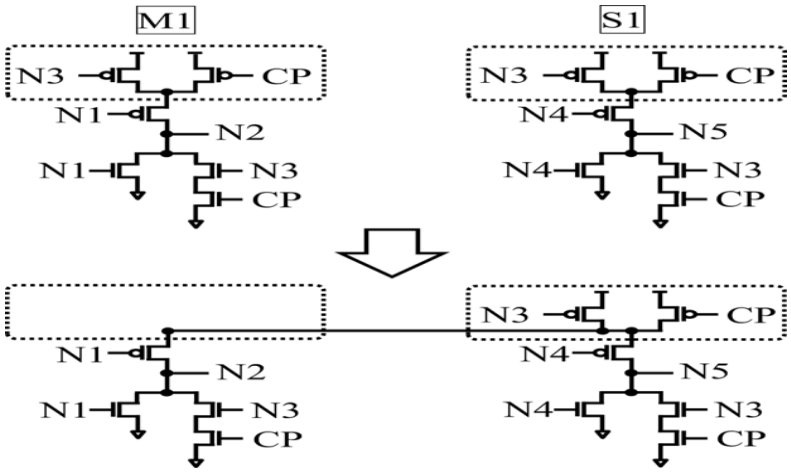

Fig. 9.Transistor merging in PMOS side

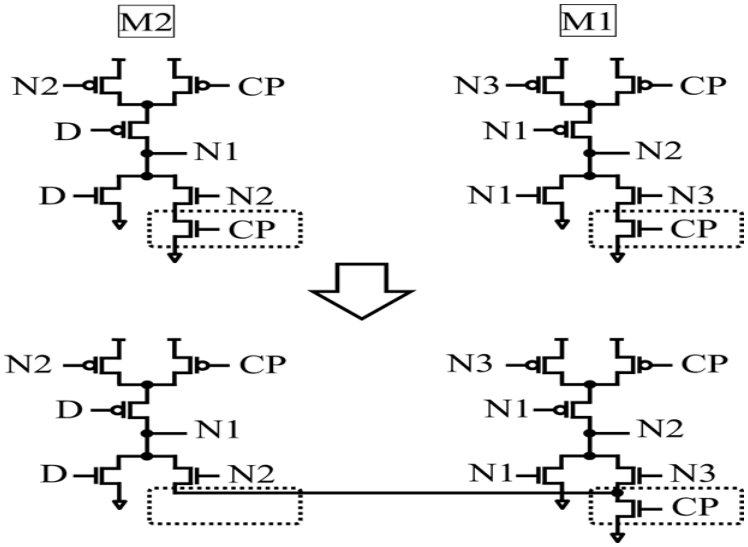

Fig. 10. Transistor merging in NMOS side

The merging process leads to the circuit shown in Fig. 11. This circuit consists of seven less transistors than the original circuit shown in Fig. 8. The number of clock-related transistors is barely three. Note that there is no dynamic circuit or pre charge circuit ,thus, no additional power dissipation emerges. We describe this reduction method Topological Compression (TC) method. The FF, TC-Method apply, is called Topologically Compressed Flip-Flop(TCFF).

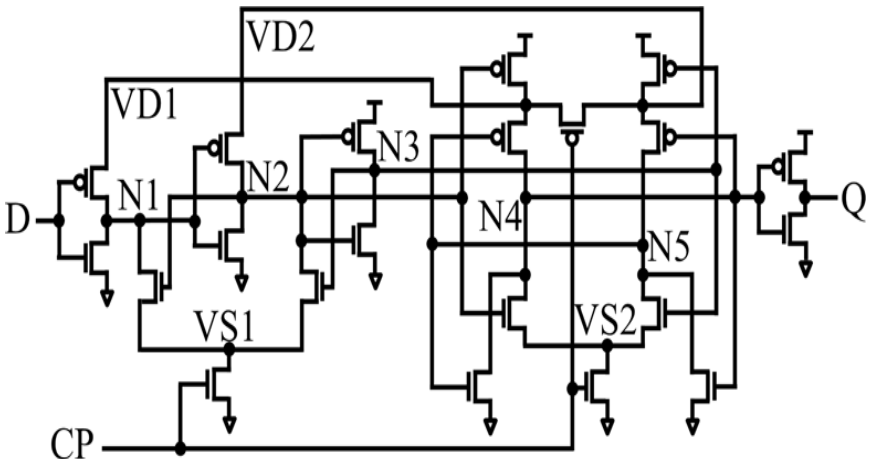

Fig. 11. Topologically compressed flip flop

For the PMOS side, two transistor pairs in M1 and S1 blocks in Fig. 9 can be shared as shown in Fig. 9. When either N3 or CP is Low, the shared widespread node becomes VDD voltage level, and N2 and N5 nodes are controlled by PMOS transistors gated N1 and N4 individually. When both N3 and CP are High, both N2 and N5 nodes are pulled down to VSS by NMOS transistors gated N2 and CP.

V. PROPOSED LOGICAL COMPRESSED PASS TRANSISTOR FLIP FLOP

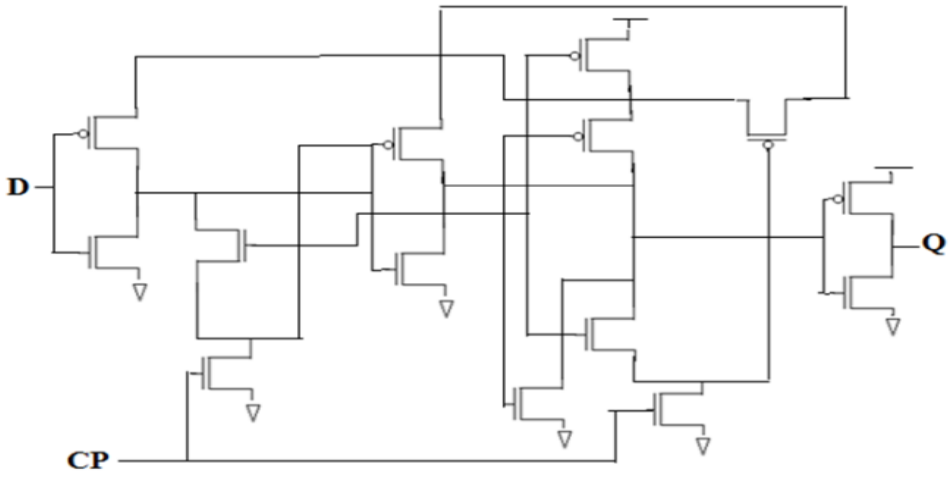

Fig. 12. Schematic diagram of LCPTL

The basic variation of pass-transistor logic compared to the CMOS logic style is that the resource side of the logic transistor networks is connected to some input signals instead of the power lines.

The advantage is that one pass-transistor network is sufficient to perform the logic operation, which results in a smaller number of transistors and smaller input loads, especially when NMOS networks are used.

TABLE I PERFORMANCE COMPARISON OF LCPTL AND OTHER FFS

S.No	Type of flip flop	Power (watts)	Delay (ns)	PDP (joules)	No of transistors
1.	CTFF	1.52-002	1.95	2.96e-02	28
2.	TCFF	1.77e-003	1.50	2.65e-03	21
3.	SCPTL	1.078e-004	2.09	2.25e-04	10

TOTAL POWER SAVING:

=(7.770e-008-3.552426e-008)

=**54%**

The power dissipation of SPTL is 54% lower than that of TCFF at 10% data activity. In the same way at 0% data activity, it is 75% lower.

Setup time is the only inferior parameter to the conventional FF, and about 70 percentages larger than the value of the conventional one. As for delay, SPTL is almost the same as the conventional FF, and better than other FFs.

For hold time, SPTL is better than the conventional FF. In summary, only setup time is large, but LCPTL keeps competitive performance to the conventional and other FFs.

VI. CONCLUSION

An extremely low-power FF, SPTL, is proposed with topological compression design methodology. LCPTL has the lowest power dissipation in almost all range of the data activity compared with other low-power FFs. The very small number of transistors, only three, connected to clock signal reduces the power drastically, and the smaller total transistor count assures the same cell area as conventional FFs.

This design is analysed in terms of power with the supposed implementation of the shift register. LCPTL has the lowest power dissipation in almost all range of the data activity compared with other low-power FFs. The power dissipation of LCPTL is 54% lower than that of TCFF at 0% data activity without area overhead. The topology of LCPTL is easily expandable to various kinds of FFs without performance penalty.

Applying to a 250 MHz experimental chip design with 40 nm technology, 98% of topologically compressed FFs are replaced by TCFFs. In a whole chip, 17% power reduction is estimated with little overhead of area and timing performance.

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